

Second Edition

Volnei A. Pedroni

Circuit Design and Simulation with VHDL



Circuit Design and Simulation with VHDL

second edition

Circuit Design and Simulation with VHDL

second edition

Volnei A. Pedroni

**The MIT Press
Cambridge, Massachusetts
London, England**

© 2010 Massachusetts Institute of Technology

All rights reserved. No part of this book may be reproduced in any form by any electronic or mechanical means (including photocopying, recording, or information storage and retrieval) without permission in writing from the publisher.

For information about special quantity discounts, please email special_sales@mitpress.mit.edu

This book was set in Times New Roman on 3B2 by Asco Typesetters, Hong Kong.
Printed and bound in the United States of America.

Library of Congress Cataloging-in-Publication Data

Pedroni, Volnei A.

Circuit design and simulation with VHDL / Volnei A. Pedroni. — 2nd ed.

p. cm.

Rev. ed. of: Circuit design with VHDL / Volnei A. Pedroni. 2004.

Includes bibliographical references and index.

ISBN 978-0-262-01433-5 (hardcover : alk. paper) 1. VHDL (Computer hardware description language).

2. Electronic circuit design. 3. System design. I. Pedroni, Volnei A. II. Title.

TK7885.7.P43 2010

621.39'5—dc22

2009045909

10 9 8 7 6 5 4 3 2 1

This second edition is dedicated to the many people, in so many countries, who made the first edition of the book so successful.

Contents

Preface	xv
1 CIRCUIT-LEVEL VHDL	1
1 Introduction	3
1.1 About VHDL	3
1.2 VHDL Versions	3
1.3 Design Flow	5
1.4 EDA Tools	5
1.5 Translation of VHDL Code into a Circuit	6
1.6 Circuit Simulation	7
1.7 VHDL Syntax	8
1.8 Number and Character Representations in VHDL	8
2 Code Structure	11
2.1 Fundamental VHDL Units	11
2.2 VHDL Libraries and Packages	11
2.3 Library/Package Declarations	13
2.4 ENTITY	14
2.5 ARCHITECTURE	16
2.6 GENERIC	17
2.7 Introductory VHDL Examples	18
2.8 Coding Guidelines	24
2.9 VHDL 2008	27
2.10 Exercises	28
3 Data Types	31
3.1 Introduction	31
3.2 VHDL Objects	31
3.3 Data-Type Libraries and Packages	36

3.4	Type Classifications	39
3.5	Standard Data Types	41
3.6	Standard-Logic Data Types	47
3.7	Unsigned and Signed Data Types	51
3.8	Fixed- and Floating-Point Types	54
3.9	Predefined Data Types Summary	59
3.10	User-Defined Scalar Types	60
3.11	User-Defined Array Types	62
3.12	Integer versus Enumerated Indexing	65
3.13	Array Slicing	66
3.14	Records	70
3.15	Subtypes	71
3.16	Specifying PORT Arrays	72
3.17	Qualified Types and Overloading	73
3.18	Type Conversion	74
3.19	Legal versus Illegal Assignments	78
3.20	ACCESS Types	79
3.21	FILE Types	80
3.22	VHDL 2008	80
3.23	Exercises	81
4	Operators and Attributes	91
4.1	Introduction	91
4.2	Predefined Operators	91
4.3	Overloaded and User-Defined Operators	98
4.4	Predefined Attributes	99
4.5	User-Defined Attributes	104
4.6	Synthesis Attributes	106
4.7	GROUP	111
4.8	ALIAS	112
4.9	VHDL 2008	114
4.10	Exercises	115
5	Concurrent Code	121
5.1	Introduction	121
5.2	Using Operators	122
5.3	The WHEN Statement	123
5.4	The SELECT Statement	124
5.5	The GENERATE Statement	129
5.6	Implementing Sequential Circuits with Concurrent Code	134

5.7	Implementing Arithmetic Circuits with Operators	135
5.8	Preventing Combinational-Logic Simplification	140
5.9	Allowing Multiple Signal Assignments	143
5.10	VHDL 2008	143
5.11	Exercises	144
6	Sequential Code	151
6.1	Introduction	151
6.2	Latches and Flip-flops	152
6.3	PROCESS	153
6.4	The IF Statement	154
6.5	The WAIT Statement	159
6.6	The LOOP Statement	161
6.7	The CASE Statement	165
6.8	CASE versus SELECT	168
6.9	Implementing Combinational Circuits with Sequential Code	169
6.10	VHDL 2008	171
6.11	Exercises	172
7	SIGNAL and VARIABLE	177
7.1	Introduction	177
7.2	SIGNAL	177
7.3	VARIABLE	178
7.4	SIGNAL versus VARIABLE	180
7.5	The Inference of Registers	185
7.6	Dual-Edge Circuits	187
7.7	Making Multiple Signal Assignments	190
7.8	Exercises	193
II	SYSTEM-LEVEL VHDL	199
8	PACKAGE and COMPONENT	201
8.1	Introduction	201
8.2	PACKAGE	201
8.3	COMPONENT	203
8.4	GENERIC MAP	208
8.5	COMPONENT Instantiation with GENERATE	211
8.6	CONFIGURATION	213
8.7	BLOCK	216
8.8	VHDL 2008	218
8.9	Exercises	219

9	FUNCTION and PROCEDURE	221
9.1	Introduction	221
9.2	The ASSERT Statement	221
9.3	FUNCTION	223
9.4	PROCEDURE	230
9.5	FUNCTION versus PROCEDURE Summary	233
9.6	Overloading	233
9.7	VHDL 2008	237
9.8	Exercises	238
10	Simulation with VHDL Testbenches	241
10.1	Introduction	241
10.2	Simulation Types	243
10.3	Writing Data to Files	245
10.4	Reading Data from Files	248
10.5	Graphical Simulation (Preparing the Design)	251
10.6	Stimulus Generation	253
10.7	General VHDL Template for Testbenches	257
10.8	Type I Testbench (Manual Functional Simulation)	258
10.9	Type II Testbench (Manual Timing Simulation)	261
10.10	Type III Testbench (Automated Functional Simulation)	261
10.11	Type IV Testbench (Automated Timing Simulation)	262
10.12	Testbenches with Record Types	264
10.13	Testbenches with Data Files	267
10.14	Exercises	271
III	EXTENDED AND ADVANCED DESIGNS	275
11	VHDL Design of State Machines	277
11.1	Introduction	277
11.2	VHDL Template for FSMs	279
11.3	Poor FSM Model	289
11.4	FSM Encoding Styles	291
11.5	The State-Bypass Problem in FSMs	292
11.6	Systematic Design Technique for Timed Machines	298
11.7	FSMs with Repetitive States	312
11.8	Other FSM Designs	312
11.9	Exercises	313
12	VHDL Design with Basic Displays	319
12.1	Introduction	319
12.2	Basic LED/SSD/LCD Driver	322

12.3	Playing with a Seven-Segment Display	327
12.4	Frequency Meter (with LCD)	330
12.5	Digital Clock (with SSDs)	337
12.6	Quick-Finger Game (with LEDs and SSDs)	340
12.7	Other Designs with Basic Displays	345
12.8	Exercises	346
13	VHDL Design of Memory Circuits	351
13.1	Introduction	351
13.2	Implementing Bidirectional Buses	352
13.3	Memory Initialization Files	353
13.4	ROM Design	357
13.5	RAM Design	362
13.6	External Memory Interfaces	368
13.7	Exercises	371
14	VHDL Design of Serial Communications Circuits	375
14.1	Introduction	375
14.2	Data Serializers/Deserializers	376
14.3	PS2 Interface	380
14.4	I ² C Interface	388
14.5	SPI Interface	399
14.6	TMDS Interface	409
14.7	Video Interfaces: VGA, DVI, and FPD-Link	419
14.8	Exercises	419
15	VHDL Design of VGA Video Interfaces	423
15.1	Introduction	423
15.2	VGA Connector	424
15.3	DDC and EDID	425
15.4	Circuit Diagram	426
15.5	Control Signals	428
15.6	Pixel Signals	429
15.7	Setup for the Experiments	430
15.8	Comments on VHDL Code for VGA Systems	430
15.9	Hardware-Generated Image	431
15.10	Image Generation with a File and On-Chip Memory	435
15.11	Arbitrary Image Generation with a File and Off-Chip Memory	438
15.12	Image Equalization with Gamma Expansion	441
15.13	Exercises	441

